REMARKS

The Office Action mailed July 19, 2002, has been received and reviewed. Claims 1 through 27 are currently pending in the application. Claims 1 through 27 stand rejected. Applicants have amended claims 1, 19 and 26. Claims 5 and 7 through 9 have been cancelled without prejudice or disclaimer, and new claims 28 and 29 have been added. Reconsideration of the application as amended herein is respectfully requested.

35 U.S.C. § 102(e) Anticipation Rejections

Anticipation Rejection Based on U.S. Patent No. 6,107,164 to Ohuchi

Claims 1 through 3, 6, 9 through 17, 23 and 26 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Ohuchi, U.S. Patent No. 6,107,164. Applicants respectfully traverse this rejection, as hereinafter set forth.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Claim 1 has been amended herein to recite the limitation of "applying an encapsulant material by transfer molding at least over substantially all of said active surface" which corresponds to a similar limitation previously recited by cancelled claim 8. Applicants respectfully submit that Ohuchi does not disclose this limitation. Rather, Ohuchi simply indicates that "the surface of the wafer ... is covered with a resin" and "the surface of the wafer 10 is sealed with a resin 23..." (col. 1, lines 48-50 and col. 3, lines 25-26). Accordingly, claim 1 is allowable over Ohuchi under the provisions of 35 U.S.C. § 102(e). It is noted that the Office has rejected the similar limitation of claim 8 as being obvious over Ohuchi because of the desirability to conformally seal the substrate within a resin. Based on the corresponding amended language of claim 1, Applicants will address this issue in the instant rejection. As used

for encapsulating semiconductors, transfer molding is typically only effected with a singulated die residing in an individual cavity. Hence, the transfer molding of an entire semiconductor substrate surface having a plurality of individual die locations is believed to be novel. Applicants respectfully submit that the Office's basis for rejecting this limitation can only be a conclusion based on the hindsight benefit of Applicants' disclosure, which is impermissible under the provisions of 35 U.S.C. § 103(a). In view thereof, Applicants respectfully submit claim 1 is allowable over Ohuchi. Claims 2, 3, 6, 10 through 17 and 23 are also allowable, among other reasons, as depending from claim 1.

Moreover, claim 11 recites "forming said intermediate conductive elements is effected by forming solder balls", claim 12 recites "forming said intermediate conductive elements is effected by forming pillars of a conductive or conductor-filled epoxy or a metal-filled elastomer" and claim 13 recites "forming said intermediate conductive elements is effected by a wire bonding capillary." Ohuchi, on the other hand describes intermediate elements as being a "post 4, composed of copper ... formed in the corresponding opening by electrolytic plating" (col. 2, lines 61-64). Also, claim 15 recites "wherein forming said external conductive elements comprises forming pillars of a conductive or conductor-filled epoxy", claim 16 recites "forming said external conductive elements comprises applying an anisotropically conductive film over said encapsulant material" and claim 17 recites "forming said encapsulant material from a material selected from the group comprising filled polymers, epoxies, silicones, silicone-carbon resins, polyimides, polyurethanes and glasses." Ohuchi fails to disclose these limitations. Accordingly, claims 11 through 13 and 15 through 17 are further allowable based on these limitations.

Claim 26 has been amended herein to be in independent form by including all of the limitations of claim 1 as originally filed. Claim 26 recites the limitations of "forming conductive traces over said encapsulant material from said exposed portions of said intermediate conductive elements to at least one channel of said pattern of channels" and "defining a peripheral edge of at least one individual die location of said plurality so as to define a plurality of laterally spaced

edge contacts." Ohuchi does not disclose any edge contacts, but rather only describes contacts for semiconductor chip 1 as being "metal electrodes 5 such as solder balls" or "layered films 13" (Figs. 5-6). Therefore Ohuchi does not describe all of the elements of claim 26, and Applicants respectfully submit it is allowable under the provisions of 35 U.S.C. § 102(e).

The rejection of claim 9 is moot, as is has been cancelled without prejudice or disclaimer.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 6,107,164 to Ohuchi

Claims 4, 5, 7 and 8 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ohuchi (U.S. Patent No. 6,107,164). Applicants respectfully traverse this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejection of claim 4 is improper because it fails to establish a prima facie case of obviousness. Amended claim 1 recites the limitation of "applying an encapsulant material by transfer molding at least over substantially all of said active surface." For the same reasons as discussed above, Ohuchi does not disclose this limitation. If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). Therefore, claim 4 is allowable over Ohuchi under the provisions of 35 U.S.C. § 103(a).

The rejection of claims 5, 7 and 8 is moot, as they have been cancelled without prejudice or disclaimer.

Obviousness Rejection Based on U.S. Patent No. 6,107,164 to Ohuchi in view of U.S. Patent No. 5,824,569 to Brooks et al. and U.S. Patent No. 5,908,317 to Heo.

Claims 15 through 22, 24, 25 and 27 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ohuchi (U.S. Patent No. 6,107,164) taken with Brooks et al. (U.S. Patent No. 5,824,569) and Heo (U.S. Patent No. 5,908,317). Applicants respectfully traverse this rejection, as hereinafter set forth.

Claims 15 through 18, 21, 22, 24 and 25 depend from claim 1. Claim 1, as amended, recites the limitation of "applying an encapsulant material by transfer molding at least over substantially all of said active surface." Neither Ohuchi, Brooks et al. nor Heo disclose this limitation, and claims 15 through 18, 22, 24 and 25 are therefore allowable as depending from claim 1.

Moreover, claim 15 recites "wherein forming said external conductive elements comprises forming pillars of a conductive or conductor-filled epoxy" and claim 16 recites "forming said external conductive elements comprises applying an anisotropically conductive film over said encapsulant material." None of Ohuchi, Brooks et al. or Heo disclose these limitations, and claims 15 and 16 are further allowable in view thereof.

Claim 19 has been amended herein to be in independent form by including all of the limitations of claim 1 as originally filed. Claims 19 recites the limitations of "providing a semiconductor substrate having an active surface including at least one layer of integrated circuitry thereon, *said active surface defining a plurality of individual die locations thereon*" (emphasis added) and "placing said semiconductor substrate with said intermediate conductive elements in alignment with conductive bumps protruding from a carrier substrate; and electrically connecting said intermediate conductive elements and said conductive bumps." Neither Ohuchi, Brooks et al. nor Heo disclose mounting a semiconductor substrate having a plurality of

individual die locations to a carrier substrate. Instead, the cited references teach singulating or dividing a substrate into individual semiconductor chips. Accordingly, claim 19 and claim 20 which depends therefrom, are allowable over Ohuchi, Brooks et al. and Heo, as these references fail to establish a *prima facie* case of obviousness.

Furthermore, claim 25 which depends from claim 1, recites the similar limitation of "placing said semiconductor substrate with said external conductive elements in alignment with terminal pads of a carrier substrate and electrically connecting said external conductive elements to said terminal pads." Accordingly, claim 25 is further allowable based on this limitation.

Claim 27 depends from claim 26. Claim 26 recites the limitations of "forming conductive traces over said encapsulant material from said exposed portions of said intermediate conductive elements to at least one channel of said pattern of channels" and "defining a peripheral edge of at least one individual die location of said plurality so as to define a plurality of laterally spaced edge contacts." Ohuchi, Brooks et al. and Heo fail to disclose any edge contacts. Claim 27 is therefore allowable as depending from claim 26. Also, claim 27 recites the limitation of "aligning said plurality of laterally spaced edge contacts with a plurality of edge connectors of a carrier substrate and electrically connecting the plurality of laterally spaced edge contacts with the plurality of edge connectors." None of the cited references disclose this limitation, and claim 27 is allowable for that reason as well.

New Claims

New claims 28 and 29 have been added to more precisely and comprehensively define the scope of the present invention, including equivalents thereof. It is respectfully submitted that claims 28 and 29 further patentably define over the references of record.

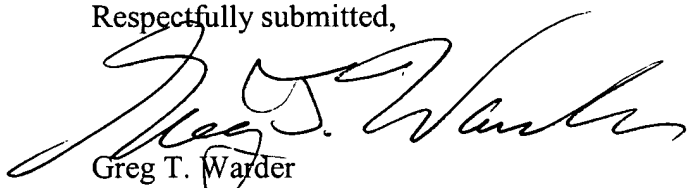
ENTRY OF AMENDMENTS

The amendments to claims 1, 19 and 26 above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application.

CONCLUSION

Claims 1 through 4, 6 and 10 through 29 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

Respectfully submitted,



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Enclosure: Version With Markings to Show Changes Made

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VERSION OF CLAIMS WITH MARKINGS TO SHOW CHANGES MADE

1. (Amended) A method of forming a semiconductor device, comprising:

providing a semiconductor substrate having an active surface including at least one layer of integrated circuitry thereon, said active surface defining a plurality of individual die locations thereon, and a plurality of bond pads associated with each of said plurality of individual die locations;

forming intermediate conductive elements over said plurality of bond pads to project a height above said active surface;

forming a pattern of mutually transverse channels in said active surface to a depth below said at least one layer of integrated circuitry, said channels circumscribing a semiconductor element location comprised of at least one individual die and exposing peripheral edges of said at least one layer of integrated circuitry;

applying an encapsulant material by transfer molding at least over substantially all of said active surface and into said channels to a depth exceeding said height of projection of said intermediate conductive elements; and

removing a depth of said encapsulant material sufficient to expose a portion of each of said intermediate conductive elements.

19. (Amended) A method of forming a semiconductor device, comprising:

providing a semiconductor substrate having an active surface including at least one layer of integrated circuitry thereon, said active surface defining a plurality of individual die locations thereon, and a plurality of bond pads associated with each of said plurality of individual die locations;

forming intermediate conductive elements over said plurality of bond pads to project a height above said active surface;

forming a pattern of mutually transverse channels in said active surface to a depth below said at least one layer of integrated circuitry, said channels circumscribing a semiconductor element location comprised of at least one individual die and exposing peripheral edges of said at least one layer of integrated circuitry;

applying an encapsulant material at least over said active surface and into said channels to a depth exceeding said height of projection of said intermediate conductive elements;

removing a depth of said encapsulant material sufficient to expose a portion of each of said intermediate conductive elements; and [The method according to claim 1, comprising:]

placing said semiconductor substrate with said intermediate conductive elements in alignment with conductive bumps protruding from a carrier substrate; and

electrically connecting said intermediate conductive elements and said conductive bumps.

26. (Twice Amended) A method of forming a semiconductor device, comprising:

providing a semiconductor substrate having an active surface including at least one layer of integrated circuitry thereon, said active surface defining a plurality of individual die locations thereon, and a plurality of bond pads associated with each of said plurality of individual die locations;

forming intermediate conductive elements over said plurality of bond pads to project a height above said active surface;

forming a pattern of mutually transverse channels in said active surface to a depth below said at least one layer of integrated circuitry, said channels circumscribing a semiconductor element location comprised of at least one individual die and exposing peripheral edges of said at least one layer of integrated circuitry;

applying an encapsulant material at least over said active surface and into said channels to a depth exceeding said height of projection of said intermediate conductive elements;

removing a depth of said encapsulant material sufficient to expose a portion of each of said intermediate conductive elements; and [The method of claim 1, further comprising]

forming conductive traces over said encapsulant material from said exposed portions of said intermediate conductive elements to at least one channel of said pattern of channels, defining a peripheral edge of at least one individual die location of said plurality so as to define a plurality of laterally spaced edge contacts therealong, and severing said semiconductor substrate in alignment with at least some of said channels including said at least one channel into a plurality of semiconductor elements each comprised of said at least one individual die location, wherein said exposed peripheral edges of said at least one layer of integrated circuitry remain covered with said encapsulant material and said plurality of laterally spaced edge contacts are located along a peripheral edge of a semiconductor element of the plurality.